CLAIMS

What is claimed is:

1. A CMOS imager system comprising:

an active pixel sensor;

a column buffer connected to the active pixel sensor; and

an analog-to-digital (A/D) converter co-located with the active pixel sensor and column buffer, such that a transmission path between the column buffer and the A/D converter acts primarily as a resistance, rather than a reactance.

2. The CMOS imager system of Claim 1, further comprising an analog programmable gain amplifier connected between the column buffer and the A/D converter, such that a transmission path between the analog programmable gain amplifier and the A/D converter acts primarily as a resistance, rather than a reactance.

3. The CMOS imager system of Claim 2, wherein the active pixel sensor comprises an access supply, a tapered reset supply and a source supply.

4. The CMOS imager system of Claim 3, wherein the A/D converter is a high-speed converter have 12 bit or greater resolution.

5. The CMOS imager system of Claim 4, wherein the column buffer has gain and fixed-pattern noise (FPN) suppression.

6. The CMOS imager system of Claim 5, wherein the analog programmable gain amplifier has tunable electronic bandwidth.

7. A digital video system comprising:

an active pixel sensor;

a column buffer connected to receive an output from the active pixel sensor;

an analog programmable gain amplifier connected to the column buffer;

an analog-to-digital (A/D) converter connected to the analog programmable gain amplifier and co-located with the active pixel sensor, column buffer and analog programmable gain amplifier, such that a transmission path between the analog gain amplifier and the A/D converter acts primarily as a resistance, rather than a reactance;

a digital programmable gain amplifier connected to an output of the A/D converter; and

a digital video interface connected to an output of the digital programmable gain amplifier.

8. The digital video system of Claim 7, wherein the active pixel sensor comprises an access supply, a tapered reset supply and a source supply.

9. The digital video system of Claim 8, wherein the A/D converter is a high-speed converter have 12 bit or greater resolution.

10. The digital video system of Claim 9, wherein the column buffer has gain and fixed-pattern noise (FPN) suppression.

11. The digital video system of Claim 10, wherein the analog programmable gain amplifier has tunable electronic bandwidth.